Amendments To The Claims

Please cancel Claim 1 without prejudice. The following list of the claims replaces all prior versions and lists of the claims in this application.

Claims 1 - 27 (Canceled).

28. (Currently amended) A capacitor structure comprising:

a storage node shape with a first portion of said storage node shape overlying a conductive via structure, wherein said ~~storage node shape~~ conductive via structure is located in an opening in an insulator layer, and wherein said conductive via structure contacts a source/drain region of an underlying metal oxide semiconductor field effect transistor (MOSFET), and wherein a second portion of said storage node shape ~~overlying~~ overlies portions of a top surface of said insulator layer; said storage node shape having alternate rows of doped regions ~~in said storage node shape~~ therein that are aligned horizontally and parallel to the top surface of said insulator layer, and having alternate rows of undoped regions ~~in said storage node shape~~ therein that are also aligned horizontally and parallel to the top surface of said insulator layer, with each set of said doped regions separated by ~~and~~ a respective one of said undoped regions; said storage node shape further having lateral grooves extending inwards from sides of each said doped region in said storage node shape, and wherein each said undoped region of said storage node shape exhibits smooth, non-groove sides;

a capacitor dielectric layer located on a smooth top surface of, and on sides of said storage node shape, and wherein said capacitor dielectric layer conforms to contours of the surfaces of the lateral grooves in each said doped region of said storage node shape; and

a conductive upper node structure located ~~overlying~~ over said capacitor dielectric layer.

29. (Previously presented) The capacitor structure of Claim 28, wherein said storage node shape is comprised of polysilicon.

30. (Previously presented) The capacitor structure of Claim 28, wherein the number of said alternate rows of doped regions is between about 3 to 10.

31. (Currently amended) The capacitor structure of Claim 28, wherein each said doped region is doped with arsenic or phosphorous ions.

32. (Currently amended) The capacitor structure of Claim 28, wherein the space between said doped regions, or the width of each said undoped region, is between about 100 to 5000 Angstroms.

33. (Currently amended) The capacitor structure of Claim 28, wherein each said lateral groove in each said doped region extends inward from the sides of said storage node structure a distance between about 50 to 500 Angstroms.

34. (Previously presented) The capacitor structure of Claim 28, wherein said capacitor dielectric layer is comprised of tantalum oxide, at a thickness between about 10 to 500 Angstroms.

35. (Previously presented) The capacitor structure of Claim 28, wherein said conductive upper node structure is comprised of polysilicon.